XII-HSC BOARD

Date : 14.03.2015 **COMPUTER SCIENCE - II (D-9) - SOLUTIONS**

1. (A)

(a) (iv) MVI A, 00H (1)

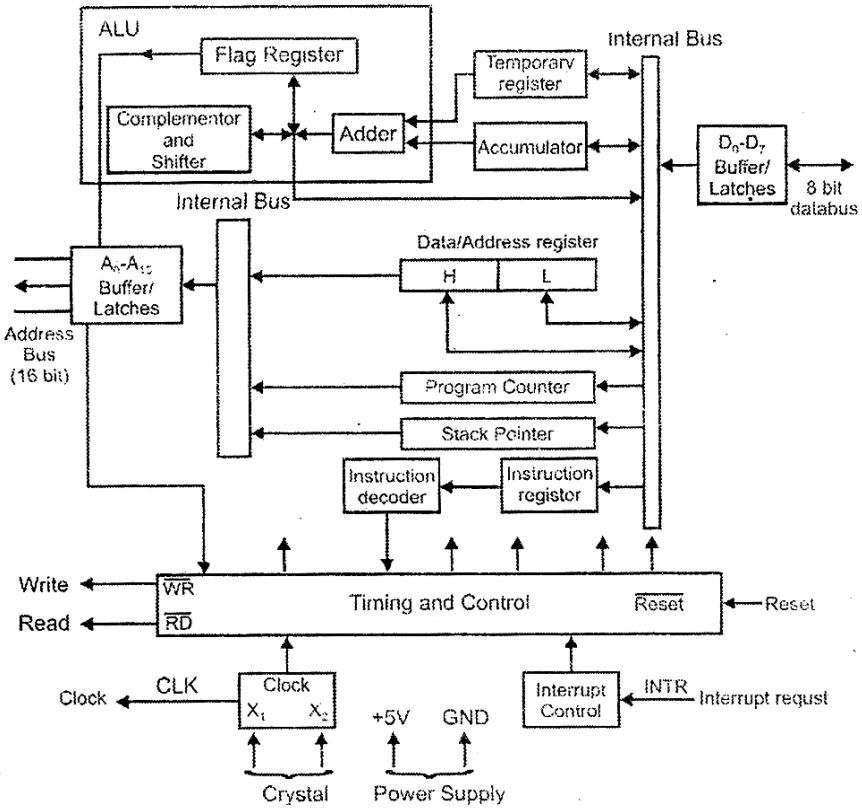
(b) (ii) 16 bit (1)

(c) (i) IR (1)

(d) (ii) REPEATER (1)

(B)

(a) Generic Microprocessor:



Block Diagram of Generic Microprocessor (3)

(b) Main Features of 8051 Microcontroller: ($^1/_2 \times 6$ pts = 3)

(1) An 8 bit ALU

(2) 4 K × 8 ROM (OR EPROM)

(3) 128 × 8 RAM

(4) Dual 16 bit timer event counter

(5) 32 I/O lines

(6) Addresses of 64 Kbytes of program memory.

(c) Hubs: (1)

(1) In some network topologies, mostly ARCNET based star topologies, a device hub is used.

(2) Hub is a connecting device in which cables can be connected without soldering wires to centralise network traffic through a single connecting point.

There are three types: (2)

(1) Active hub (2) Passive hub (3) Switching hub

Active hub : interconnect the network and also amplifies the signal received apart from splitting and retransmitting it to the destination.

Passive hub : It only splits and transmits signal received and it can not amplify it. This do not contian any electronic component.

Switching hub : This quickly routes the signals between ports of hubs. It can be used in place of router.

2. (A)

(a) (1) Microprocess 8085 has 8-bit **data bus** and 16-bit **address bus**. ($^1/_2 \times 6$ pts = 3)

(2) The least significant 8-bits of address bus are passed on the same eight lines as that of data bus i.e. on the signal lines $AD_7 - AD_0$.

(3) These signal lines are bi-directional.

(4) They are used for dual purpose for lower order 8-bit of address and as well as 8-bit of data. This is known as multiplexing and such bus is known as multiplexed bus.

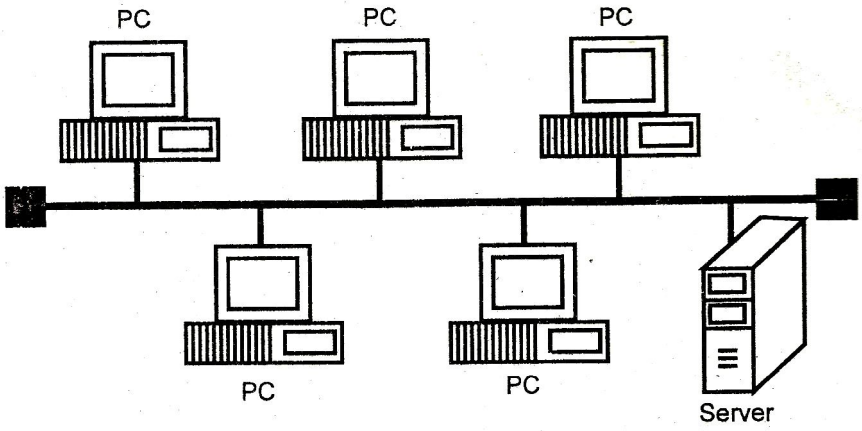
(5) In multiplexed means, first to select one and then other.

(6) In executing an instruction, during earlier part of cycle these lines are used as the lower order address bus. During label part of cycle, these lines are used as data bus.

(b) BUS Topology : ($1\ ^1/_2$)

(1) In a BUS physical topology, all the devices are connected to a common shared cable, called as backbone of the network.

(2) A BUS physical topology is shown in following figure :



(3) The bus is available for each node to send its data to each and every computer node.

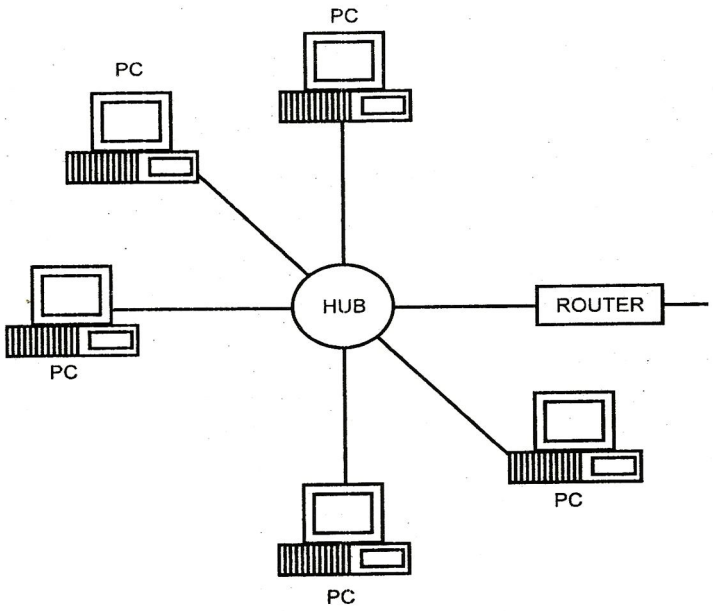
STAR Topology: ($1\frac{1}{2}$)

(1) In a STAR topology all the workstations are connected to central hub.

(2) The hub receives signal from a workstation and routes it to the proper destination.

(3) STAR physical topology is often implemented to implement BUS or RING logical topology.

(4) A STAR topology is shown in following figure:



(c) Arithmetical Instructions: ($1\frac{1}{2}$)

(1) **ADD r : [ADD REGISTER]**

Format : $[A] \leftarrow [A] + [r]$

Addressing : Register addressing

Group : Arithmetic group

Bytes : 1 byte

Flag : All

(2) **ADI data : [ADD IMMEDIATE TO ACCUMULATOR]**

Format : $[A] \leftarrow [A] + \text{data}\ (\text{byte } 2)$

Addressing : Immediate addressing

Group : Arithmetic group

Bytes : 2 bytes

Flag : All

(3) **SUB r : [SUBTRACT REGISTER FROM ACCUMULATOR]**

Format : $[A] \leftarrow [A] - [r]$

Addressing : Register addressing

Group : Arithmetic instructions group

Bytes : 1 byte

Flag : All

Logical Instructions : $(1\frac{1}{2})$

(1) **ANA r** : **[LOGICAL AND WITH ACCUMULATOR]**

Format : $[A] \leftarrow [A] \wedge [r]$

Addressing : Register addressing

Group : Logical group

Bytes : 1 byte

Flag : S, Z, P are modified Cy = 0, Ac = 1

(2) **ANI data** : **[ADD IMMEDIATE WITH ACCUMULATOR]**

Format : $[A] \leftarrow [A] \wedge$ data

Addressing : Immediate addressing

Group : Logical group

Bytes : 2 bytes

Flag : S, Z, P are modified Cy = 0, Ac = 1

(3) **ORA M** : **[LOGICAL OR WITH MEMORY]**

Format : $[A] \leftarrow [A] \vee [[H][L]]$

Addressing : Register Indirect

Group : Logical group

Bytes : 1 byte

Flag : S, Z, P are modified Ac and Cy are rest

(B)

(a) (1) 8085 provides 5 hardware interrupts: (1)

(i) TRAP (ii) RST 7.5 (ii) RST 6.5 (iv) RST 5.5 (v) INTR

(2) These interrupts are vectored interrupts. It means that when these interrupts are given , it is directed (or vectored) to transfer the control to specific memory location given by

TRAP $= 4.5 \times 8 = 0024$ H RST $7.5 = 7.5 \times 8 = 003$C H

RST $6.5 = 6.5 \times 8 = 0034$ H RST $5.5 = 5.5 \times 8 = 002$C H

(3) Among these interrupts, TRAP is non- maskable interrupt which can not be disabled. But the other four interrupts are maskable interrupts, which can be disabled.

(4) The TRAP has highest priority and the INTR has lowest priority among the hardware interrupts. The hardware interrupts in descending order of priority are listed below:

(i) TRAP - highest priority (ii) RST 7.5

(iii) RST 6.5 (iv) RST 5.5

(v) INTR - lowest priority. (3)

(b) (i) MOV B, M : [MOVE FROM MEMORY] (1)

Format : $[B] \leftarrow [[H] - [L]]$

Addressing : Register Indirect addressing
Group : Data transfer group
Bytes : 1 byte
Flag : None

(ii) ADC C : [ADD REGISTER TO ACCUMULATOR WITH CARRY] (1)

Format : $[A] \leftarrow [A] + [C] + [Cy]$

Addressing : Register addressing
Group : Arithmetic group
Bytes : 1 byte
Flag : All

(iii) SPHL : [MOVE HL TO SP] (1)

Format : $[SP_L] \leftarrow [L]$

$[SP_H] \leftarrow [H]$

Addressing : Register addressing
Group : Machine control group [stack operation]
Bytes : 1 byte
Flag : None

(iv) XCHG: [EXCHANGE H AND L WITH D AND E] (1)

Format : $[H] \leftrightarrow [D]$
$[L] \leftrightarrow [E]$

Addressing : Register
Group : Data transfer group
Bytes : 1 byte
Flag : None

3. (A)

(a) Microcontroller is a Single Chip Computer. This is used for dedicated functions. (1)

Advantages: (2)

(1) It can be used as independent controllers in various machines.

(2) It includes all the essentials of a computer on a single chip like CPU, R/W memory, ROM it can be used as a microcomputer.

(3) It reduces the cost of a system than microprocessor based system. So it can be used in low cost products like toys.

(b) (1) Dual Pipelining : (1)

The use of super scalar architecture incorporates a dual- pipelining in Pentium processor, which lets Pentium to process more than one instruction per clock cycle and achieve a high level of performance.

(2) Branch Prediction: (1)

(i) The advantage of branch prediction is that, using it, the Pentium makes an educated guess where the next instruction following a conditional instruction will be.

(ii) This prevents the instruction cache from running dry during conditional instruction.

(3) On chip changes : (1)

The data and code on-chip caches improves the processing speed of the Pentium processor.

(4) 64-Bit Data Bus :

(i) Pentium has 64 bit data bus which allows higher speed of data transfer to it.

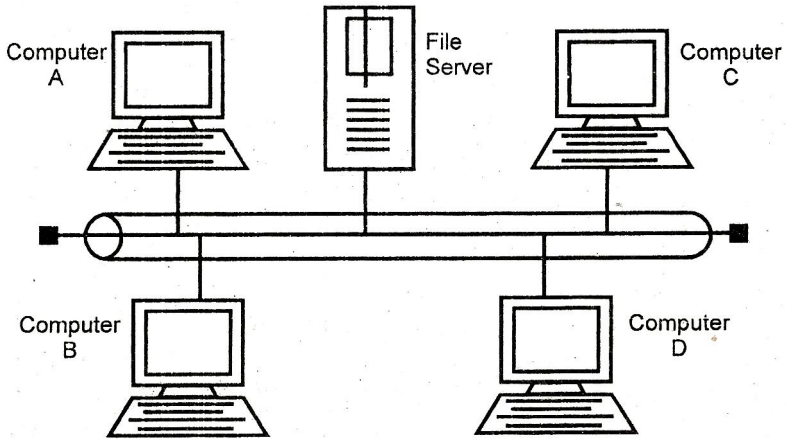
(ii) The data transfer speed of pentium is twice as fast as a processor with 32-bit data bus.

(c) (1) Ethernet devices are connected to a common shared medium that provides the path along which the electronic signals will travel. Historically, this medium was co-axial cable. But now-a-days twisted pair cable or fibre optic cable are also used.

(2) Ethernet network transmit data in small units called **frames**.

(3) Each frame must contain source address as well as destination address, which identifies recepient and sender of message. The address will uniquely identify node. No two Ethernet devices can have same address.

(4) Ethernet network is as shown in following figure.



In above figure when computer A sends message to computer C, computers B and D will also get the message and check whether the diestinations address matches to its own address or not, if not, it will discard the frame. (3)

(B)

(a) PUSH-PUSH REGISTER PAIR ON STACK (2)

This is a single byte instruction. The contents of the register pair specified in the operand are copied into the stack.

(1) The stack pointer is decremented and the contents of higher order register in pair (such as B in BC pair, D in DE pair) are copied on stack.

(2) The stack pointer is decremented again and contents of lower order register are copied on the stack. No flags are modified. Contents of register pair are unchanged.

Example:

PUSH D

Will push contents of DE pair

Let D = 15 H & E = 23 H

Let SP = 2300 H

Then after executing PUSH D we will get following contents in SP and stack.

SP = 22 FE	STACK
22 FE	23H
22FF	15H
2300	

← SP

POP–POP OFF STACK TO REGISTER PAIR (2)

This is single byte instruction. On execution copies two top bytes on stack to designated register pair in operand.

(1) Contents of top most location of stack called stack top are copied into lower register (such as C in BC etc) of the pair. The SP is incremented by 1.

(2) Contents of the stack location pointed by SP are copied into higher register of the pair. The stack pointer SP is incremented by 1. No flags are affected. Contents of stack are unchanged.

Example:

Consider SP = 22FE H with following contents stored on stack.

On execution of instruction POP H the contents of H, L, SP will be as shown in figure.

SP = 22 FE	STACK
22FE	10H
22FF	24H
2300	

← SP

BEFORE EXECUTION

SP = 2300	STACK
22FE	10H
22FF	24H
2300	

← SP

H = 24 H L = 10 H

AFTER EXECUTION

(b) 8085 has five flags. Sign flag, zero flag, Auxiliary carry flag, Parity flag and Carry flag. A 8-bit register is used to represent five flags as shown in following figure.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
S	Z	–	Ac	–	P	–	Cy	Status flags

Bit number

Where S - Sign flag, Z- Zero flag, Ac- Auxiliary carry flag,
P - Parity flag, Cy- Carry flag.

(1) Sign flag (S) : (1)

After the execution of arithmetic and logic operation, if the most signification of the result is 1, then the flag is set to 1 otherwise 0.

This flag is used with signed number. If MSB is 1, the number will be negative and if it is 0, the number will be positive.

(2) Zero flag(Z) : (1)

After performing an arithmetic or logic operations, if the result is zero, then zero flag is set to 1, else it is reset. This flag is modified by the results in accumulator as well as in other registers.

(3) Auxiliary carry flag(Ac) : (1)

In an arithmetic operation, when carry is generated from bit D_3 to D_4, the auxiliary carry flag is set to 1. This flag is only available internally and used for B.C.D. operations and not available for programmer.

(4) Parity flag (P) : (1)

Parity flag is set to 1, if the result stored in accumulator contains even parity, i.e., even number of 1's. If accumulator contains odd number of 1's, the flag is 0.

4. (A)

(a) (i) **$\overline{\text{INTA}}$** (1)

(1) $\overline{\text{INTA}}$ is an Abbrevation for interrupt acknowledgment.

(2) A low an $\overline{\text{INTA}}$ indicates that the processor has acknowledged an INTR interrupt.

(ii) **IO/$\overline{\text{M}}$** (1)

(1) It is status signal indicates whether the address bus is for I/O device or for memory.

(2) When it goes high, the address ont he address bus referring I/O device and when it goes low, the address on the address bus referring memory.

(iii) **$\overline{\text{RD}}$** (1)

(1) This is read control signal. This is active low signal.

(2) This signal indicates that selected I/O or memory device is to be read and data is available.

(b) (1) Microcontroller is a single chip microcomputer.

(2) They are used as independent controllers in machined or as slaves in distributed processing.

(3) They are used as machine tools, chemical processors, medical instrumentation and sophisticated guidance control.

(4) Some applications require simple timing and bit set/ reset functions; other require high speed data processing capability.

(5) Many low cost products such as electronic toys, microwave ovens, VCRs are base on microcontrollers.

(6) A home security system, a tape deck and intelligent multimeter can also be build by using microcontroller. ($^1/_2 \times 6$ pts = 3)

(c) Twisted Pair Cable: ($1\,^1/_2$)

(1) It consists of a pair of wires or one or more pairs of two twiseted copper wires insulation.

(2) This is inexpensive medium.

(3) EMI effect is maximum.

Coaxial Cable: ($1\,^1/_2$)

(1) It is a hallow cable with a solid copper at the center of the cable surrounded by plastic from.

(2) Relatively expensive i.e. twice or thrice than twisted pair.

(B)

(a) (i) **T-States :** (1)

The subdivision of an operation, which is performed in one clock period is called as T-state.

(ii) **Machine Cycle:** (1)

Machine cycle is defined as the time required to complete any operation of accessing wither memory or I/O which is the subpart of an instruction.

(iii) **Instruction Cycle:** (1)

An instruction cycle is defined as the time required to complete the execution of an instruction. The 8085 instruction cycle consists of one to five machine cycle.

(iv) **FETCH Cycle : This question is out of syllabus so student will get bonus marks for this.**

(b) (i) Fiber optic cable if cable is broke, still Data Transfer is possible, while in electrical cable its not possible.

(ii) In fiber optics cable, Data transfer is optically using light rays while in electrical cable, data transfer is done by electricity.

(iii) In fiber optic cable, data rate is very high in terms of gbps, while in electrical cable, its data rate is very low in terms of mbps.

(iv) Cost of fiber optic cable is very high while, in electric at cable its very low.

(4)

5. (a)

Mnemonics		Comment
Opcode	Operand	
MVI	A, 00	; Store 00 to Acc
MOV	D, A	; Store 00 to D Reg
LXI	H, 8085	; Reg 8085 in HL pair
MOV	B, M	; store content of Memory to B Reg
MVI	C, 09	; Store count in C Register
BACK: ADD	B	; Addition of B reg with Acc.
JNC	: NEXT	; Jump if Cy ? 0, go to next
INR	D	; Increment D Reg. by 1
NEXT : DCR	C	; Decrement counter by 1
JNZ	: BACK	; Jump C ? 0; go to Back
INX	H	; Increment HL pair by 1
MOV	M, A	; Result stored from Acc. to memory
INX	H	; Increment HL pair by 1
MOV	M, D	; Store D reg to memory
RST	1.0	; Restart.

(5)

(b)

Mnemonics		Comment
Opcode	**Operand**	
MOV A, E		; Copy E content to Accumulator
CMA		; Compliment Accumulator
MOV L, A		; Copy Accumulator to L Register
MOV A, D		; Copy D content to Accumulator
CMA		; Compliment Accumulator
MOV H, A		; Copy Acc. to HL Pair
INX H		; Increment HL pair by 1
RST 1.0		; Restart.

(5)

(c)

Mnemonics		Comment
Opcode	**Operand**	
MVI C, 0A		; Block length in C Register
LXI H, 2050		; Store 2050 in HL pair
MOV A, M		; Copy content of memory to Acc.
BACK: INX H		; Increment HL pair by 1
CMP M		; Compare Acc. with memory
JC : NEXT		; If Cy = 1, then go to NEXT
MOV A, M		; Copy content of Memory to Acc.
NEXT : DCR C		; Decrement C Reg. by 1
JNZ : BACK		; If Cy ? 0, then go to Back
INX H		; Increment HL by 1
MOV M, A		; Store Acc. content to memory
RST 1.0		; Restart.

(5)

OR

(a)

Mnemonics		Comment
Opcode	**Operand**	
LXI H, 8081		; Store 8081 in HL Pair.
MVI C, 14 H		; Store count in C Register.
MVI A, BCH		; Store BC_H in Accumulator .
BACK : MOV M, A		; Copy Acc content to memory.
INX H		; Increment HL pair by 1.
DCR C		; Decrement C Reg by 1.
JNZ : BACK		; If C ? 0 then go to BACK.
RST 1.0		; Restart.

(5)

(b)

Mnemonics		Comment
Opcode	Operand	
MVI C, 00		; Store 00 in C Register
LXI H, 6067		; Store 6067 in HL pair
MOV A, M		; Copy memory to Acc.
INX H		; Increment HL pair by 1
MOV B, M		; Copy memory to B Register
BACK: CMP B		; Compare Acc. with B Register
JC : NEXT		; If Cy = 1, go to next
SUB B		; Subtract B from Acc.
INR C		; Increment C content by 1
JMP : BACK		; Jump to Back
INX H		; Increment HL pair by 1
MOV M, C		; Store Quotient in memory
INX H		; Increment HL pair by 1
MOV M, A		; Store Reminder in memory
RST 1.0		; Restart.

(5)

(c)

Mnemonics		Comment
Opcode	Operand	
LIX H, $20F9_H$		; Store 20F9 in HL pair
MOV A, M		; Copy memory data to Acc.
ANI OF		; Logically And Acc. with 0F
MOV B, A		; Copy Acc. to B Reg
MOV A, M		; Copy memory content to Acc
ANI F0		; Logically And Acc. with F0
RRC		; Rotate digits
RRC		; Rotate digits
RRC		; Rotate digits
RRC		; Rotate digits
CMP B		; Compare Acc. with B reg.
JNZ : NEXT		; If A ? B; go to next
MVI B, 00		; Store 00 in B reg.
RST 1.0		; Restart.
NEXT : MVI B, FF		; Store FF in B reg.
RST 1.0		; Restart.

(5)